In the Claims

Amend the claims as follows:

1. (Original) A latch device having a variable resistive trip point, comprising:

a voltage source;

an adjustable trip point current reference;

a latch circuit having a fuse latch output; and

a trip point control element, said trip point control element being operable to control the amount of current passing through said latch circuit based on said adjustable trip point current reference that is compensated by a latch mimic circuit.

2. (Original) The latch device as set forth in claim 1, wherein said trip point control element is a transistor, and wherein a gate of said transistor is connected to said adjustable trip point current reference that is compensated by a latch mimic circuit.

3. (Original) The latch device as set forth in claim 2, wherein said transistor has a source connected to said voltage source and a drain connected to said latch circuit, wherein a change in said adjustable trip point current reference changes an amount of current flowing through said transistor into said latch circuit.

4. (Original) The latch device as set forth in claim 1, including a feedback circuit to determine the reference current that will make the latch input voltage equal to the latch-inverter trip point.

5. (Original) The latch device as set forth in claim 4, wherein the latch mimic circuit receives the reference current and the latch voltage is monitored by a differential amplifier.

6. (Currently Amended) The latch device as set forth in claim 5, wherein ~~said fuse element~~

~~is~~ an antifuse element is coupled to the latch device.

7. (Currently Amended) The latch device as set forth in claim 1, wherein said adjustable trip point current reference ~~is adjustable binarily~~ further comprises a weighted binary adjustment circuit.

8. (Original) The latch device as set forth in claim 1, further comprising a trip point current reference circuit for developing said adjustable trip point current reference, said trip point current reference circuit having a plurality of selectable inputs for changing the adjustable trip point current reference.

9. (Currently Amended) The latch device as set forth in claim 8, wherein said plurality of inputs are connected to ~~binarily weighted~~ a plurality of reference transistors ~~which are operable~~ configured to ~~change~~ produce a binary weighted adjustment of the ~~adjustable~~ trip point current reference ~~binarily~~.

10. (Original) The latch device as set forth in claim 1, further comprising a trip point current reference circuit for developing said adjustable trip point current reference using a current mirror control.

11. (Currently Amended) The latch device as set forth in claim 15, wherein said latch circuit has a polling transistor comprising a source, a drain and a gate, the gate being connected to a strobe signal input, said polling transistor being operable to poll a fuse connected to the latch circuit when the strobe signal input is in an active state.

12. (Original) The latch device as set forth in claim 11, further comprising a trip point current reference circuit for developing said adjustable trip point current reference, and wherein said strobe signal input is connected to a bypass transistor in said trip point current reference circuit to adjust said adjustable trip point current reference to a state in which said trip point control

element allows a maximum amount of current to pass from said voltage source into said latch circuit when said strobe signal input is in its inactive state.

13. (Original) The latch device as set forth in claim 1, further comprising a trip point current reference circuit for developing said adjustable trip point current reference, said trip point current reference circuit comprising a bandgap current reference.

14. (Currently Amended) The latch device as set forth in claim 15, wherein said trip point control element is operable to provide the latch device with at least a first trip point for testing a resistance margin of a fuse element, a second trip point for improving soft error immunity, and a third trip point for normal operation.

15. (Currently Amended) A latch device having a variable resistive trip point, comprising:

a voltage source;

an adjustable trip point current reference;

a latch circuit having a fuse latch output;

a trip point control element, said trip point control element being operable to control the amount of current passing through said latch circuit based on said adjustable trip point current reference that is compensated by a latch mimic circuit; and

~~The latch device as set forth in claim 1 which includes~~ a buffered latch to prevent creep up from altering the switch point of the latch output.

16. (Original) The latch device of claim 15 wherein at least one buffer stage is inserted between an input inverter of the fuse latch and its feedback devices.

17. (Original) The latch device as set forth in claim 15 wherein the reference current is compensated for process, voltage or temperature.

18. (Currently Amended) A latch device having a variable resistive trip point comprising:

a voltage source;

~~an adjustable trip point current source;~~

a latch circuit having a fuse latch;

a trip point control means to control the current passing through a fuse coupled to the latch circuit;

~~a compensation means for adjusting the trip point current reference; and~~

~~a means for compensating the current reference for changes in process, voltage or temperature to maintain a constant resistive trip point~~

a compensated current source adapted to adjust for variation of a trip point voltage of the fuse latch caused by variations in manufacturing process and operating temperature and voltage; and

a voltage mimic circuit and operational amplifier coupled to the fuse latch to adjust the fuse latch trip point voltage.

19. (Original) A method to control a variable resistive trip point fuse latch having a plurality of fuse elements with differing states comprising:

determining the state of the fuse elements;

storing the state of the fuse elements;

selecting a predetermined fuse element; and

compensating the trip point current reference based on a mimic circuit.

20. (Original) The method of claim 19 in which the mimic circuit is compensated based on changes in process, voltage, or temperature.